REMARKS

This Amendment is responsive to the Office Action dated May 17, 2006. Claims 1 – 11 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kozlowski (U.S. Patent No. 6,493,030). Additionally, two informalities with Claim 11 were noted.

With respect to Claim 11, the applicant has amended "column" to "row" as suggested. However, "the improvement" language has not been changed. This is standard "Jepson"-style claim language (See 37 CFR 1.75(e)(2)).

Claim 1 has been amended to include language that the access supply is a current source which operates a distributed feedback amplifier when connected to the MOSFETs, as described in the specification on page 7. Claims 8 and 11 similarly describe the access supply as comprising a distributed feedback amplifier.

In contrast, Kozlowski '030 does NOT disclose an access supply comprising a distributed feedback amplifier and/or that the access supply is a current source. Vdd 22 is simply a standard voltage supply. The office action cites Fig. 7, and col. 6, lines 35 – 54 as further supporting the rejection that the access supply is a distributed feedback amplifier. However, Fig. 7 and related description are describing the source supply 30 and not an access supply connected as required in the present claims.

Forming an access supply as a distributed feedback amplifier has the advantage of providing increased gain over the circuit illustrated in the '030 patent (which lacks an access supply comprising a distributed feedback amplifier). Thus, the present claims are allowable over the cited reference.

The Applicant also wishes to point out the circuit disclosed in U.S. Patent No. 6,697,111. This circuit illustrates an access supply 40 connected to a row bus 22.

However, this circuit lacks an access MOSFET as required by the present claims. Moreover, it would not be obvious to simply combine the circuits of '030 and '111. In '030, the circuit strictly operates access MOSFET 20 as a switch and relies only on the basic gain of the CMOS inverter amplifier to enable noise suppression. It is not obvious to one skilled in the art to boost the gain of the CMOS inverter amplifier by operating MOSFET 20 as a cascade because of the overt danger in causing the amplifier to oscillate and the uncertainty in achieving uniform noise suppression.

By way of further background, Kozlowski in L.J. Kozlowski, G. Rossi, L. Blanquart, R. Marchesini, Y. Huang, G. Chow and J. Richardson, "Pixel Noise Suppression via SoC Management of Tapered Reset in a 1920x1080 CMOS Image Sensor," JSSCC, Vol. 40, No. 12, Dec. 2005, pp. 2766-2776 (copy enclosed) notes that the resonant frequency for the distributed amplifier at high gain, such as for the case of a cascoded amplifier is:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{R_{sw}C_oC_1(1+b)}}$$

Consequently, calculations in Table II of this reference show that achieving good noise reduction requires relatively long reset times (i.e., long time constants) and low quality factors that result in resonant frequencies of tens of MHz. One consequence is the possibility that the imaging sensor's clock frequency is now close to the circuit resonant frequency, thereby increasing risk of extremely high noise due to the attendant SoC circuit oscillation.

The other result is that switch resistance on the order of tens of GW must be supported on a uniform basis across the imaging sensor. It is not obvious to one skilled

in the art that such uniformity in subthreshold operation is achievable using conventional CMOS processes.

If the Examiner believes that a telephone conference will expedite the prosecution of this case, the Examiner is encouraged to contact the undersigned attorney at the below-listed number.

The Commissioner is hereby authorized to charge any fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR §1.78 to Deposit Account No. 50-2603, **referencing Attorney Docket No. 359999.01300**. **A duplicate sheet is attached**.

Respectfully submitted,

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Dated: September 18, 2006

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as Express mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, US Patent & Trademark Office, Alexandria, VA 22313-1450, on September 18, 2006.

Dated: September 18, 2006

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Maryalice Kelley

Pixel Noise Suppression via SoC Management of Tapered Reset in a 1920×1080 CMOS Image Sensor

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***Abstract*—Correlated double sampling is widely used in imaging arrays to eliminate noise generated when a CCD's sense capacitance or a CMOS sensor's photodiode is reset after signal integration and readout. Instead, we suppress photodiode kTC noise using a SoC implementation for progressive reset; supporting SoC components include a feedback amplifier having elements distributed amongst the pixel and column buffer, a tapered reset clock waveform, and reset timing generator. The reset method does not swell pixel area, compel processing of the correlated reset and signal values, or require additional memory. Theoretical analysis is presented along with experimental results. Integrated in a 1920 by 1080 imager having 5 μm by 5 μm pixels in 0.25-μm CMOS, measured random noise for 5.5-fF detector capacitance is ~8 e− to 225 MHz video rate with image lag <0.12%. Random noise of ~30 e− is otherwise predicted and achieved using conventional reset. Sensor S/N ratio with progressive readout is ≥52 dB at 60 Hz and 72 Hz frame rate.**

***Index Terms*—Active pixel sensor, CMOS image sensor, kTC noise.**

I. Introduction

IMAGE sensor suitability for each camera application is judged by weighing key metrics including optical format, pixel count, sensitivity, video rate, dynamic range, and noise (fixed and random). These factors can be mutually exclusive so that some specifications are favored over others when designing a sensor for a specific use. We discuss theoretical background and experimental results for a system-on-chip (SoC) solution that leverages CMOS integration to minimize optical format and noise, even at high video rates, while simultaneously maximizing sensitivity, pixel count, and dynamic range.

Today's CCD and CMOS imaging sensors mainly use correlated double sampling (CDS) [1] to eliminate kTC noise and suppress 1/f noise. CDS is especially effective for CCD-based cameras since the composite (signal plus reset) and reset levels are collocated in the serial video stream; hardware implementation cost is low to subtract each pixel's correlated noise component in real time. CDS can nevertheless boost total noise since its usage doubles CCD video bandwidth even when amplifier thermal noise may already dominate [2], [3]. This excess noise is problematic for emerging applications including high-definition television (HDTV; ≥74.25 MHz video) [4] and multimegapixel digital still cameras (DSC) supporting image capture in rapid bursts. The latter currently distribute the video stream to several output taps, each operating at ~30 MHz, to tame excess noise.

CMOS imaging sensors also use CDS, but with major architectural alteration—differencing is executed prior to the video output driver. Some sensors apply CDS in each pixel [5]; others process in buffers supporting each column (i.e., column buffer) [6]; and a few subtract reset and signal frames in the camera electronics. Astronomers, for example, capture series of nondestructive frames during each integration epoch to build very low noise images on a pixel-by-pixel basis. The so-called Fowler sampling [7] achieves lower random noise than CDS, but requires extensive camera post-processing. In-pixel CDS uses valuable real estate that can instead be used for maximizing signal pickup and saturation charge. Column-wise and camera-based schemes for implementing post-pixel CDS can greatly complicate signal processing requirements.

II. SoC Noise Suppression

The many forms of imaging sensors matriculate to two basic types, depending upon whether signal amplification is performed at each pixel or outside the pixel array. By having amplification at each pixel, active pixel sensors enhance signal transfer and sensitivity. Passive-pixel sensors conversely boast simple pixels that maximize fill factor. Both classes share common row and/or column buses for pixel read and reset; a column buffer usually services all the pixels common to the vertical bus in both types.

Fig. 1 shows the basic SoC architecture the active pixel sensor of this study. Noise suppression is implemented by augmenting the three transistors in the pixel with additional components in the column buffer. The distributed components alternately constitute a source follower amplifier during pixel readout and a single-stage amplifier with feedback capacitor and reset switch having variable resistance during pixel reset. The number of pixel transistors is minimized and thus optical fill factor maximized. This paper focuses on the distributed feedback amplifier and its efficacy in progressively resetting each pixel using a tapered reset clock that is tailored to extinguish reset noise and limit mode-switching noise.

III. Theoretical Analysis of Reset Noise

In this section, we summarize the theoretical analysis of reset noise on a capacitive node that is connected to a single-stage feedback amplifier through a variable resistor. The latter acts as the reset switch wherein a tapered reset clock supervises

Manuscript received April 15, 2005; revised July 15, 2005.

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Digital Object Identifier 10.1109/JSSC.2005.858480

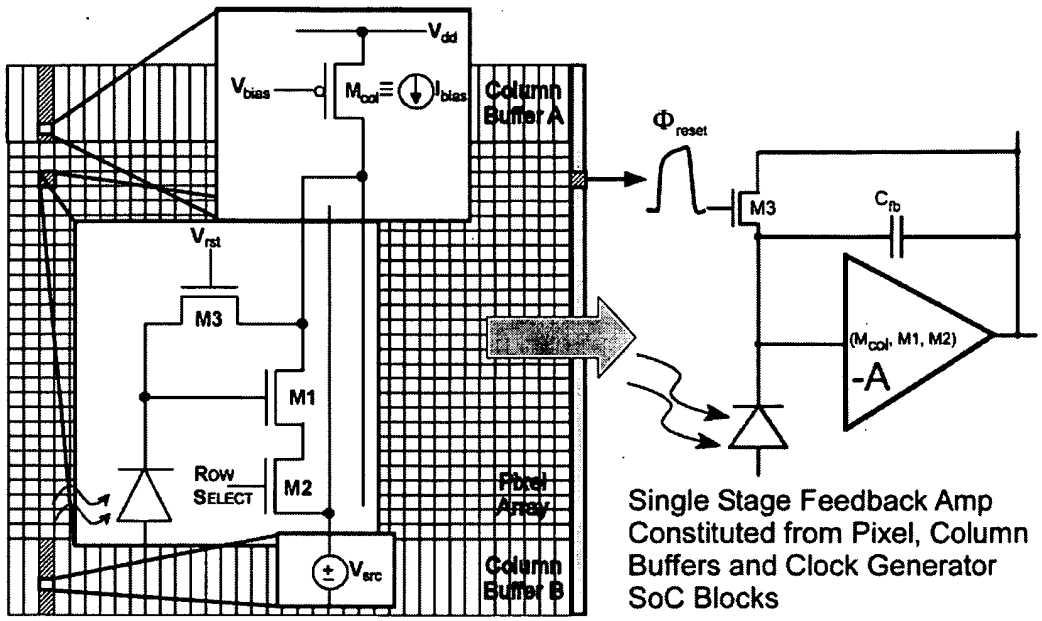

Fig. 1. System-on-chip feedback amplifier for noise suppression.

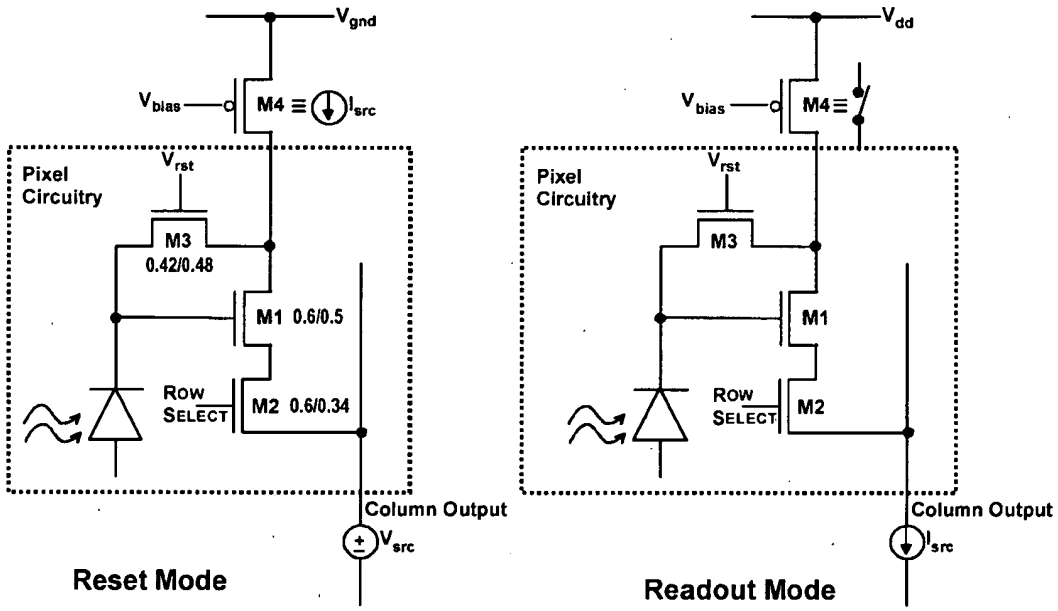

Fig. 2. CMOS amplifier with suppressed kTC noise and progressive readout: (a) in reset; (b) during readout.

its variable resistance. One application is CMOS active pixel sensors (APS) requiring small pixels having high sensitivity, high optical fill factor, and low noise. We use the distributed single-stage feedback amplifier formed from the transistors in the pixel and in the column buffer to reduce photodiode kTC noise and simplify active pixel design. A key objective of the analysis is a simple expression for predicting noise to allow intuitive design.

A. Active Pixel Design

Fig. 2(a) and (b) illustrates the progressive readout scheme for reset and readout. Fig. 2(a) is a transistor level diagram for pixel reset; the pixel consists entirely of n-type MOSFETs and an n-type photodiode in a p-substrate. In reset mode, M4 acts as a current source set by $V_{\rm bias}$, M1 acts as a transconductance, and M3 acts as a variable resistance $R_{\rm sw}$, controlled by $V_{\rm rst}$. The series resistance of M3 must be increased gradually by a slowly decreasing $V_{\rm rst}$ ramp, which is common to all pixels being reset, to enable the feedback transconductance of M1 to null the reset noise. Here, M2 is conducting ("row select" is high) and the output column must be tied to a low impedance voltage source. This type of array can reset (i.e., integration then starts) within an aperture on the order of microseconds. Fig. 2(b) shows the same pixel, but in the readout mode. To read out, $V_{\rm bias}$ is simply brought down to turn M4 on harder, so it acts like a closed

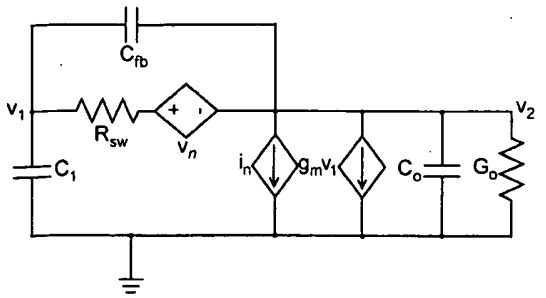

Fig. 3. Equivalent noise model for tapered reset operation.

switch, and so that M1 has power to operate as a source follower with current source in the column buffer outside of the imaging array.

The pixel thus physically reduces to the compact three-transistor (3T) layout used for the classical source follower per detector [8]. The concomitant tradeoffs of the distributed configuration include the facts that the amplifier output node sees the entire column capacitance and that only one row can be reset at a time. Also, just after the reset process starts by enabling M3 (i.e., in a given row), small parasitic leakages or subthreshold current tails can charge the parasitic capacitances associated with the M1–M2 interfaces of all other rows. This scheme nevertheless reduces pixel fixed-pattern offsets, because the photodiode node charges to a voltage that cancels M1 variations. Even long rows are resettable within several tens of microseconds for largest noise reduction.

Topologically, the scheme is similar to a distributed capacitive transimpedance amplifier (CTIA) readout [9], but without the explicit feedback capacitor. It is also similar to Fowler's active reset having the reset amplifier collocated within each pixel [10].

B. Noise Model

Fig. 3 shows the small-signal circuit model during reset, which we call tapered reset since noise suppression involves tapering the reset waveform to enable active feedback and minimize generation of excess noise [11]. This model is used to calculate the steady-state noise envelope at the reset node corresponding to a fixed value of the reset switch resistance $R_{\rm sw}$. It is the envelope reached after all transients have decayed. Of course, this is not quite the real situation and is only the first step to study the decay rate of the transients and dependence on $R_{\rm sw}$. The objective is to ultimately design an appropriate waveform for $V_{\rm rst}$. If $V_{\rm rst}$ ramps down at a slow rate, it might take too long to reset the array or one of its rows. If $V_{\rm rst}$ ramps down too quickly, the initially large kTC noise envelope will not sufficiently decay before the switch opens completely. The process hence involves "bandwidth control noise suppression" [12].

The photodiode node has voltage v_1 and capacitance C_1 to ground. The amplifier output node has voltage v_2, output capacitance C_o and output conductance G_o to ground. C_o is the capacitance associated with the M1–M3–M4 junction in the pixel and the entire reset access bus, most of which comes from the M1–M3 junctions of all the rows. g_m is the transconductance of M1, possibly degenerated by M2; it is shown as a controlled current source. The feedback capacitance $C_{\rm fb}$ is normally a parasitic or could include a separate component. Noise from M1 is represented by current source i_n, and noise from M3 (which is in the ohmic region) is represented by voltage source v_n.

This model excludes noise from capacitive feedthrough of $V_{\rm rst}$. We also note that we do not consider the impact of CMOS distributed channel resistance; while it does not appear in standard noise models for FETs in saturation, it is still physically coupled to C_1 through the gate capacitance. Finally, we also do not consider excess noise coupled onto C_1 via $C_{\rm fb}$, which is manageable by considering pixel layout and clock transitions.

C. Transfer Function

We first calculate the transfer function for the voltage on the reset node, v_1. This will approximate the variance of charge trapped at the node, under the conditions during readout. The reader will note that this assumes a very small value for $C_{\rm fb}$ because the amplifier output node, v_2, will have its own variance (i.e., at the end of the reset period). The advantage of looking at v_1 is that a closed-form expression is available for the thermal noise, which is important for insight. Also, the analysis is extended to rigorously include the effect of $C_{\rm fb}$, and while no closed-form expression has been derived, it is possible to get an upper bound for the noise. Equation (1) shows the transfer function with $v_n(s)$ and $i_n(s)$ as inputs, and $v_1(s)$ as the output. This result corresponds exactly to the model of Fig. 3 with no approximations made.

$$\frac{v_1(s)}{} = \frac{[(G_o+sC_o)v_n(s)-(1+sR_{\rm sw}C_{\rm fb})i_n(s)]}{\left[\begin{array}{c}(R_{\rm sw}\,(C_oC_1+C_{\rm fb}(C_o+C_1)))s^2+\\ (Co+(1+R_{\rm sw}G_o)C_1+R_{\rm sw}(G_o+g_m)C_{\rm fb})s+(G_o+g_m)\end{array}\right]}. \tag{1}$$

D. Key Equations

Equation (2) is the noise envelope integral, using the general form of $H(s)$. The power spectrum integral reduces to terms involving normalized integrals. By using standard definitions of the quality factor and resonant frequency (angular), a boxed formula for the noise envelope follows. At this stage, the only assumption is that the system is not degenerate: it has a defined q.f. > 0.

$$H(s) = \frac{E+Fs}{As^2+Bs+C}$$

$$\downarrow$$

$$\int_0^\infty |H(j\omega)|^2\,d\omega = \left(\frac{E}{C}\right)^2 \omega_0 \int_0^\infty \frac{1}{(1-u^2)^2+\frac{u^2}{\text{q.f.}^2}}du + \left(\frac{F\omega_0}{C}\right)^2 \omega_0 \int_0^\infty \frac{u^2}{(1-u^2)^2+\frac{u^2}{\text{q.f.}^2}}du$$

$$\downarrow$$

$$\omega_0 = \sqrt{\frac{C}{A}}$$

$$\text{q.f.} = \sqrt{\frac{AC}{B}}$$

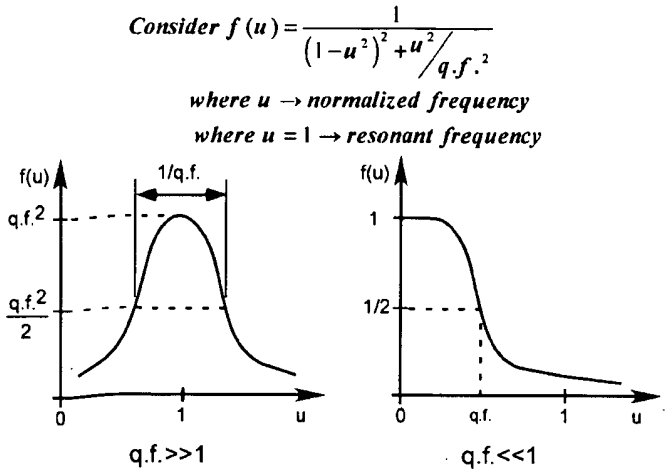

Fig. 4. Quality factor and $f(u)$.

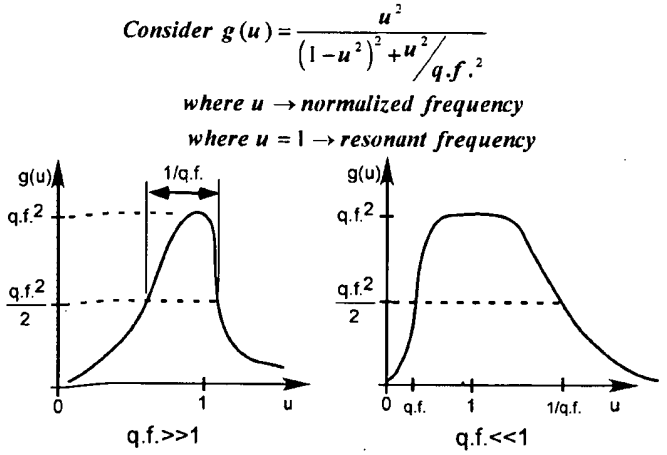

Fig. 5. Quality factor and $g(u)$.

$$\downarrow$$

$$\frac{1}{2\pi}\int_0^\infty |H(j\omega)|^2\, d\omega = \frac{E^2}{4CB} + \frac{F^2}{4AB}. \tag{2}$$

Equations (3a)–(3d) are the formulas needed for deriving the reset noise envelope. Two integrals, in normalized form, appear with the parameter q.f., which stands for "quality factor," as in classic treatments of second-order systems. Sketches of the two integrands are shown in Figs. 4 and 5 for very small and very large values of q.f. While not needed for white noise calculations, these sketches aid 1/f noise calculations. The expressions for thermal noise from the two FETs sized for identical transconductance and for the reset switch thermal noise are both spectral densities referred to Hz. (This assumes, reasonably, that both FETs are in saturation. If the g_m of the current source FET differs from that of M1, a fudge factor can be used.)

$$\int_0^\infty f(u)du = \frac{\pi}{2}(\text{q.f.}), \text{ where}$$

$$f(u) = \frac{1}{(1-u^2)^2 + \dfrac{u^2}{\text{q.f.}^2}} \tag{3a}$$

$$\int_0^\infty g(u)du = \frac{\pi}{2}(\text{q.f.}), \text{ where}$$

$$g(u) = \frac{u^2}{(1-u^2)^2 + \dfrac{u^2}{\text{q.f.}^2}} \tag{3b}$$

$$i_n^2 = \frac{4}{3}(4kT)g_m \quad \text{(two FETs)} \tag{3c}$$

$$v_n^2 = 4kTR_{\text{sw}} \quad \text{(reset FET)}. \tag{3d}$$

E. Expression for Noise Envelope

The closed-form results will be for thermal (i.e., Johnson) noise only. Flicker noise is discussed later. To directly apply (2) and (3) to the transfer function of (1), i_n and v_n must be treated individually. They can then be added in the power domain, i.e., quadratically, because the sources v_n and i_n are independent. Also, after calculating v_1 noise, it can be put in terms of a "noise equivalent capacitance," C_{equiv}. For $C_{\text{equiv}} < C_1$, the circuit effectively suppresses reset noise (in term of electrons) relative to the detector-limited kTC noise level. By inverting the traditional kTC formula for charge power noise, a C_{equiv} giving the correct charge noise can be found because

$$C_{\text{equiv}} = \frac{Q_I^2}{kT} = \frac{C_1^2 V_I^2}{kT}. \tag{4}$$

The solution for C_{equiv}, shown in (5) at the bottom of the page, has four components. The two "switch terms" are from the reset switch (M3), and the two "amp. terms" are from the amplifier. Moreover, the two left terms come from the $f(u)$ integrand, and the two right terms come from the $g(u)$ integrand. (This identification is needed for 1/f noise fudge factors.) The only

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$$\text{if } A_{\text{dc}} \gg 1, \text{ then } C_{\text{equiv}} = \text{switch terms} + \text{amp terms, where}$$

$$\text{switch terms: } \frac{K_1 C_1}{A_{\text{dc}}(I + K_1 + K_2)} + \frac{\frac{C_0 C_1}{(C_0 + C_1)}}{(1+b)(I + K_1 + K_2)}$$

$$\text{amp terms: } \underbrace{\frac{4}{3}\frac{C_1}{C_0 + C_1}\frac{C_1}{A_{\text{dc}}(I + K_1 + K_2)}}_{f(u)\text{ terms}} + \underbrace{\frac{4}{3}\frac{C_1}{C_0 + C_1}\frac{bK_2 C_1}{(1+b)(I + K_1 + K_2)}}_{g(u)\text{ terms}} \tag{5}$$

approximation so far is amp DC gain, $A_{\rm dc}$, much greater than unity ($1 + A_{\rm dc}^{-1} \approx 1$), as was used in simplifying some denominator terms. This closed-form solution is for the steady-state noise envelope at a fixed value of $R_{\rm sw}$, which manifests itself in the values of K_1 and K_2. Equation (6) defines dimensionless parameters $A_{\rm dc}$, b, K_1, and K_2:

$$\begin{aligned} A_{\rm dc} &= \frac{g_m}{G_0} \quad \text{(dc gain)} \\ b &= \frac{C_{\rm fb}(C_0 + C_1)}{C_0 C_1} \\ K_1 &= \frac{R_{\rm sw} G_0 C_1}{C_0 + C_1} \\ K_2 &= \frac{R_{\rm sw} g_m C_{\rm fb}}{C_0 + C_1}. \end{aligned} \tag{6}$$

We now compute the rate of envelope decay for the second-order system. When underdamped or critically damped, the time constant of the (exponential) decay envelope is given as the tentative value, $\tau_{\rm tent}$, in (7). There are two decay rate modes when overdamped and the longest is used here; both situations are covered in the last formula. It is not 100% rigorous to use results from a time-invariant system and apply them to a time-varying system (we are varying $R_{\rm sw}$), but both thinking in terms of Lyapunov theory [13] (where a dynamic system is critically appraised for divergence and sensitivity to initial conditions) or energy functions in the time domain, and because the $R_{\rm sw}$ variation does not add "energy," this approach should be adequate. As stated earlier, the switch's channel capacitance is not modeled here. Equation (8) is the resonant frequency, f_o, in hertz and is useful for extending the analysis to include 1/f noise.

Noise Envelope Decay (RMS)

if $A_{\rm dc} \gg 1$, then:

$$\begin{aligned} \text{q.f.}^2 &= \frac{K_2(1+b)}{b(1+K_1+K_2)^2} \\ \tau_{\rm tent} &= 2R_{\rm sw}\left(\frac{C_o C_1}{C_o + C_1}\right)\left(\frac{1+b}{1+K_1+K_2}\right) \end{aligned} \tag{7}$$

$$\tau = \begin{cases} \tau_{\rm tent}, & (\text{q.f.})^2 \geq 1/4 \\ \dfrac{\tau_{\rm tent}}{1 - \sqrt{1 - 4(\text{q.f.})^2}}, & (\text{q.f.})^2 < 1/4 \end{cases}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{g_m}{R_{\rm sw} C_o C_1 (1+b)}}. \tag{8}$$

F. Large $C_{\rm fb}$ Case

The above calculation looked only at Q_1 and did not consider the effect of the noise on the other side of $C_{\rm fb}$, which is typically held at a fixed voltage during readout. Equation (9) shows the noise equivalent charge trapped on the node. A simple upper bound is derived without recomputing the new transfer function by referring back to (5) with its four terms. We separate $C_{\rm equiv}$ into $C_{\rm sw}$ and $C_{\rm amp}$ terms. Note that the $g(u)$ term in $C_{\rm amp}$ is dropped. Instead, it manifests itself as a term equivalent to a first-order RC low-pass filter with $C_{\rm fb}$, which has a kTC noise envelope. The triangle inequality is used to give the upper bound at the bottom of (10). This result is good for any value of $C_{\rm fb}$; it does not require that $C_{\rm fb}$ actually be "large" compared to something. Also, note that the decay rate result is still valid.

Noise Equivalent Charge for Large $C_{\rm fb}$:

Using $Q = C_1 V_1 + C_{\rm fb}(V_1 - V_2)$

$$C_{\rm sw} = \frac{K_1 C_1}{A_{\rm dc}(1+K_1+K_2)} + \frac{\left[\frac{C_0 C_1}{(C_0+C_1)}\right]}{(1+b)(1+K_1+K_2)}$$

$$\text{and} \quad C_{\rm amp} = \frac{4}{3}\left(\frac{C_1}{C_0+C_1}\right)\frac{C_1}{(1+K_1+K_2)}$$

$$\therefore\ C_{\rm equiv} \leq C_{\rm amp} + C_{\rm sw} + C_{\rm fb} + 2\sqrt{C_{\rm sw} C_{\rm fb}}. \tag{9}$$

G. Simplified Noise Expression

Equation (10) is the simplified expression for the rms noise charge, Q_n, (not noise power) involving two terms. The first is kTC noise from the photodiode node capacitance C_1, with reduction factor $1/(1+K_1+K_2)$ and ensuing noise charge (Q_1). The second term is noise from $C_{\rm fb}$. We assume that $A_{\rm dc}$ is high so that the first term of $C_{\rm sw}$ is negligible. Later, numerical examples will validate this assumption and DC gain term contribution.

Simplified Reset Noise Approximation:

- Assume $A_{\rm dc} \gg 1$.
- Combine the second $C_{\rm sw}$ term with $C_{\rm amp}$ while dropping 4/3 term and noting that
  $$C_{\rm sw} + C_{\rm amp} \cong \frac{C_1}{(1+K_1+K_2)}.$$
- Use $\sqrt{C_{\rm sw} C_{\rm fb}} \leq \sqrt{(C_{\rm sw} + C_{\rm amp}) C_{\rm fb}}$.
- Simplify bound on $C_{\rm equiv}$ for large $C_{\rm fb}$ to get rms noise expression
  $$Q_n \cong \sqrt{kT(C_{\rm amp} + C_{\rm sw})} + \sqrt{kTC_{\rm fb}}$$
  or
  $$Q_n \cong \sqrt{\frac{kTC_1}{(1+K_1+K_2)}} + \sqrt{kTC_{\rm fb}}. \tag{10}$$

H. Key Observations

Significant noise reduction occurs for $K_1 + K_2$ much greater than unity, as seen when we refer back to the definitions in (5) and note that $K_1 + K_2$ is proportional to $R_{\rm sw}$. Also, there are two ways to raise its coefficient to extract more noise reduction out of the same $R_{\rm sw}$ for fixed g_m:

1) increase the output conductance (lower the DC gain);
2) increase the feedback capacitance.

In a globally resettable array where p-MOSFETn $M_{\rm col}$ is included at each pixel site rather than at the column buffer, each pixel amplifier likely operates subthreshold to keep total power at a reasonable level. This gives a very low G_o. In fact, g_m could be about 1000 G_o, and hence $C_{\rm fb}$ would be key to improving noise reduction (i.e., K_2 would dominate the effect).

In a progressive row reset array, on the other hand, the designer can add G_o to the output node (as it is a column bus), and does not have to rely on $C_{\rm fb}$.

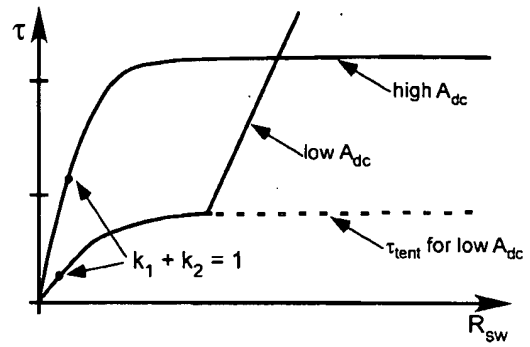

Fig. 6. Envelope decay versus switch resistance R_{sw}.

TABLE I
SAMPLE CALCULATIONS FOR GLOBAL RESET EXAMPLE

g_m=0.1 μS, G_o=10^{-4} μS, A_{dc}=1000, C_1=20 fF, C_0=10 fF, C_{fb}=0.5 fF

f_0(MHz)	R_{sw}(GΩ)	K_1+K_2	C_{equiv}(fF)	τ_{tent}(μs)	q.f.^{2}	τ (μs)
340	0.1	0.167	17	1.2	1.8	1.2
240	0.2	0.333	15	2.1	2.7	2.1
150	0.5	0.834	11	3.8	3.6	3.8
110	1.0	1.67	7.5	5.2	3.4	5.2
76	2.0	3.33	4.6	6.5	2.6	6.5
48	5.0	8.34	2.1	7.5	1.4	7.5
34	10	16.7	1.1	7.9	0.8	7.9
24	20	33.3	0.6	8.2	0.4	8.2
15	50	83.4	0.2	8.3	0.17	19

The decay time constant is an issue with regard to the coefficient on R_{sw} for $K_1 + K_2$. Fig. 6 shows what happens at different G_o values, or DC gains (e.g., in a progressive row reset design). By lowering the DC gain, we get more noise reduction at lower R_{sw} along with shorter time constant, particularly the tentative time constant. However, the potential drawback is that q.f. $= 1/2$ at a "modest" value of $K_1 + K_2$, and the actual time constant rises very rapidly for increasing R_{sw}. On the other hand, for high A_{dc}, the time constant is longer, yet the circuit can handle a much larger value of $K_1 + K_2$ before the "q.f. breakover" point. [See (7).] q.f. can be low for very low values of R_{sw}. Finally, note that this tradeoff would not change if C_{fb} were instead increased.

I. Numerical Examples and Practical Considerations

To help illustrate the qualitative tradeoffs discussed in the last section, it is necessary to show some numerical examples before continuing the discussion. Four cases are presented, all of which correspond to the first term in the formula of (10); i.e., a simplified C_{equiv}. The C_{fb} term is omitted to aid its comparison with the "main" C_1 term.

Table I lists sample parameter values that could be expected in a global reset array having four transistors in each pixel including p-type MOSFET M4 so that all pixels are simultaneously resettable, rather than progressively reset (row-by-row) using the distributed amplifier setup. Note the very low g_m, which is from an NFET biased at a few nanoamperes, and high A_{dc}. Also, C_o represents a small junction capacitance, and C_1 a relatively large photodiode capacitance for a pixel with high optical fill factor. The feedback capacitance is in the order of the gate overlap capacitance, perhaps a little higher, in case a "supplement" is added for better parameter control.

TABLE II
SAMPLE CALCULATIONS FOR DISTRIBUTED RESET EXAMPLE

g_m=40 μS, G_o=0.08 μS, A_{dc}=500, C_1=10 fF, C_0=3.0 pF, C_{fb}=0.3 fF

f_0(MHz)	R_{sw}(GΩ)	K_1+K_2	C_{equiv}(fF)	τ_{tent}(μs)	q.f.^{2}	τ (μs)
570	0.1	0.167	7.0	1.4	6.6	1.4
400	0.2	0.333	5.4	2.2	8.0	2.2
250	0.5	0.834	3.2	3.2	7.1	3.2
180	1.0	1.67	1.9	3.8	4.8	3.8
130	2.0	3.33	1.0	4.2	3.0	4.2
80	5.0	8.34	0.4	4.5	1.4	4.5
57	10	16.7	0.2	4.5	0.70	4.5
40	20	33.3	0.1	4.6	0.37	4.6
25	50	83.4	0.05	4.7	0.15	13

The table shows that about 1 GΩ is needed to stimulate significant noise reduction, i.e., we see C_{equiv} is dropping to 1/100th of C_1, the detector capacitance. In the absence of noise abatement, the dominant noise for the 3T pixel in electrons is, theoretically, $\sqrt{\mathbf{kTC_1}}/\mathbf{q}$, so a C_{equiv} that is 100× smaller compared to C_1 effectively lowers noise 10×.

Circuit efficacy for noise reduction improves with increasing R_{sw}. At $R_{sw} \sim 20$ GΩ, C_{equiv} reduces to the order of C_{fb}, beyond which the noise reduction benefit diminishes rapidly. It is easy to verify that K_2 is the dominant term. Also, remember the first term of C_{sw} that was left from the simple formula. No matter what is done with other parameters, A_{dc} limits this term to 0.02 fF, which is definitely negligible. The time constant is several microseconds, and a few tens of microseconds are needed for $\sim$ 10× noise reduction where C_{equiv} is about 1/100th of the detector capacitance, C_1.

Table II shows an example with distributed (progressive) reset, with the high DC gain expected of an amplifier operated near the FET threshold. This is for a slightly smaller photodiode, an imaging array with hundreds of rows (thereby increasing C_o), a high bias current of few microamps, and no C_{fb} supplement. R_{sw} about 1 GΩ is still needed here for effective noise suppression, but higher g_m makes smaller R_{sw} somewhat more effective than before. The C_{fb} term, K_2, still dominates, and C_{equiv} approaches C_{fb} at $R_{sw} > 5$ GΩ and $\sim$ 10× noise reduction is again possible.

Table III shows another example for distributed reset. The assumptions are similar here, except for higher G_o (and hence lower A_{dc}). 10× noise reduction is now achieved at lower R_{sw} with shorter time constant. Note that the time constant shoots up at a lower noise reduction factor since K_1 now dominates, but significant noise reduction is still tenable. However, the C_{sw} term that was earlier considered insignificant, $K_1C_1/A_{dc}(1 + K_1 + K_2)$, is now 0.25 fF at $R_{sw} = 2$ GΩ. In other words, there are now two more factors "creeping" into the total noise: C_{fb}, which was also in the earlier example, and the "A_{dc} term" of the original C_{sw} expression. These factors increase the key time constants and the potential for picking up 1/f noise.

It is difficult in the prior three examples to give an exact figure for the expected noise performance in term of electrons because of the differing envelope decay rates and other factors such as (post-pixel) readout noise. Yet the following rule of thumb can be put forward. It should be possible, in most cases, to achieve

TABLE III
SAMPLE CALCULATIONS FOR DISTRIBUTED RESET WITH LOWERED AMPLIFIER GAIN, A_{dc}

g_m=40 μS, G_o=3 μS, A_{dc}=14, C_1=10 fF, C_0=3.0 pF, C_{fb}=0.3 fF

f_o(MHz)	R_{sw}(GΩ)	K_1+K_2	C_{equiv}(fF)	τ_{tent}(μs)	q.f.^{2}	τ (μs)
570	0.1	1.4	4.2	0.83	2.4	0.8
400	0.2	2.8	2.6	1.0	1.9	1.0
250	0.5	7.0	1.2	1.2	1.1	1.2
180	1.0	14	0.67	1.3	0.6	1.3
130	2.0	28	0.34	1.4	0.32	1.4
80	5.0	70	0.14	1.4	0.13	4.5
57	10	140	0.07	1.4	0.068	9.5
40	20	280	0.04	1.4	0.034	20
25	50	700	0.02	1.4	0.014	49

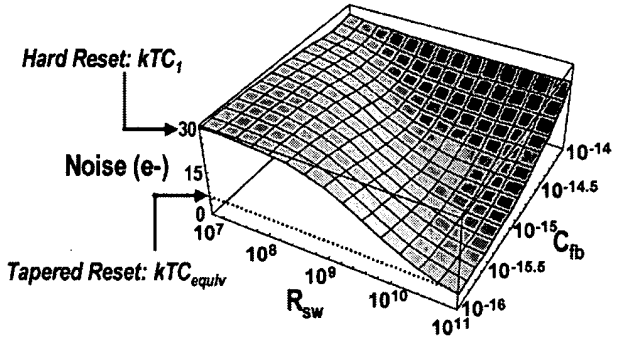

Fig. 7. Predicted random noise versus C_{fb} and R_{sw} for C_1 = 5.5 fF and HDTV readout.

random noise ≤10 e−, as this corresponds to kTC noise for several fF capacitance, such as for 3T pixels having ≤ 5 μm pixel pitch. Achieving random noise significantly below 10 e− is feasible with higher difficulty since there is a practical limit for fabricating manageable C_{fb}. Further noise reduction below 5 e− also leaves less headroom for other readout noise since the noise voltage is dropping to very low levels.

When considering 1/f noise, for example for the amplifier term, it is possible to use the resonant frequency f_o (at the far left in the tables) as the frequency at which $u = 1$ in the integrand in Fig. 3 to numerically apply a fudge factor to its corresponding integral. As q.f. and f_o change due to R_{sw}, the shape of the integrand and the normalized 1/f corner frequency change, so that numerical integration may be needed for each value. However, if one verifies that both f_o and q.f. decrease as R_{sw} increases, at a given 1/f corner the highest or worst case fudge factor occurs toward the end of the tapered reset period. In other words and as expected, although efficacy of noise reduction increases with longer reset time, integrated 1/f noise adds to the total noise.

Table IV shows the last example. Here we are resetting a large capacitance, such as the bus in a passive pixel sensor, using an amplifier at each column. Such passive sensors were used in early CMOS products so it is instructive to highlight a major difference between this situation and active pixels. The large g_m, low A_{de}, and modest C_o and C_{fb} values are to be expected from a simple column-based feedback amp. Studying the same simplified C_{equiv} expression, we find is negligible and K_1 now dominates. R_{sw} is now in the kΩ range, and q.f. is very low; it is a heavily damped system. The time constant is short and we approach 10× noise reduction at R_{sw} of only 1 GΩ. However,

TABLE IV
SAMPLE CALCULATIONS FOR COLUMN BUS RESET EXAMPLE

g_m=500μS, G_o=100μS, A_{dc}=5, C_1=5.0pF, C_0=50fF, C_{fb}=2fF

f_o(MHz)	R_{sw} (kΩ)	K_1+K_2	C_{equiv}(fF)	τ_{tent}(μs)	q.f.^{2}	τ (μs)
220	1.0	0.1	4500	9.1×10^{-5}	8.3×10^{-4}	0.055
160	2.0	0.2	4200	1.7×10^{-4}	1.4×10^{-3}	0.061
98	5.0	0.5	3300	3.3×10^{-4}	2.2×10^{-3}	0.075
70	10	1.0	2500	5.0×10^{-4}	2.5×10^{-3}	0.10
49	20	2.0	1650	6.7×10^{-4}	2.2×10^{-3}	0.15
31	50	5.0	830	9.1×10^{-4}	1.4×10^{-3}	0.30
22	100	10	450	8.3×10^{-4}	8.3×10^{-4}	0.55
16	16	20	240	9.5×10^{-4}	4.5×10^{-4}	1.1
10	500	50	98	9.8×10^{-4}	1.9×10^{-4}	2.6
7	1000	100	50	9.9×10^{-4}	9.8×10^{-5}	5.1

the omitted C_{sw} term, $K_1C_1/A_{de}(1+K_1+K_2)$, is now 1.0 pF for all $K_1(K_1+K_2)$ much greater than unity. In other words, omitting the C_{sw} term in the equivalent noise capacitance is valid for active pixel sensors with global and progressive row reset, but not for passive pixel sensors.

J. Conclusion

In the context of active reset feedback circuitry for APS sensors, whether self-contained in the pixel or distributed along a column bus, reset noise can be minimized without using correlated double sampling by appropriately tuning reset switch resistance, feedback capacitance, and amplifier output conductance (for low DC gain) at reset times appropriate for video imaging.

The available reset time for HDTV, for example, is ∼ 20 μs for progressively imaging 1920 by 1080 format at 60 Hz frame rate. Extending the noise analysis using graphical means, Fig. 7 shows the parametric tradeoff gamut for achieving reset noise ≥ 3× below the kTC level at reset time on the order of 10 μs. Specifically, assuming detector capacitance of 5.5 fF and conservative values for amplifier parameters (R_{sw} > 10 GΩ at C_{fb} < 1 fF), reset noise lowers to ≤10 e− from the normally expected kTC level of 30 e−. Increasing R_{sw} to over 50 GΩ at C_{fb} ∼ 0.1 fF lowers reset noise significantly below 10 e−.

IV. HDTV SENSOR PERFORMANCE

Tapered reset efficacy was studied in a CMOS imaging-SoC (iSoC) sensor specifically designed for high definition television. The sensor floor plan is shown in Fig. 8. Having die size of 13.1 mm by 9.3 mm in 0.25-μm process technology, the iSoC comprises a 1920 by 1080 array of three-transistor pixels with 5 μm by 5 μm area, upper and lower banks of analog buffers reading each sensor column, digital signal processing including line-mixing and pixel-binning, pipeline 12-bit digitization, programmable state machine and bias generator, and three banks of dual-port SRAM totaling 6 kB. The pipeline ADC has 7-stage configuration (3-3-3-3-3-2-2) with error correction, is distributed at sensor top and bottom, and consumes ∼0.1 pJ/DN at 74.25 MHz sampling rate.

Analog signal processing includes offset correction and programmable gain amplifiers in the column buffers and at the ADC input, black-level clamp, dynamic noise reduction via threshold-programmable analog gain management in the

TABLE V
PREDICTED AND MEASURED PIXEL NOISE FOR 1920 × 1080 CMOS SENSOR

Reset Mode	Predicted Pixel Noise (e-)	Measured Pixel Noise (e-)	Image Lag (%)
Hard Reset (C_1=5.5fF)	30.4	29	0.1
Hard + Soft Reset	<15	13	0.2
Soft Reset	<15	5	1.5
Tapered Reset	<10	8	0.1
Tapered Reset II	<10	3	0.2

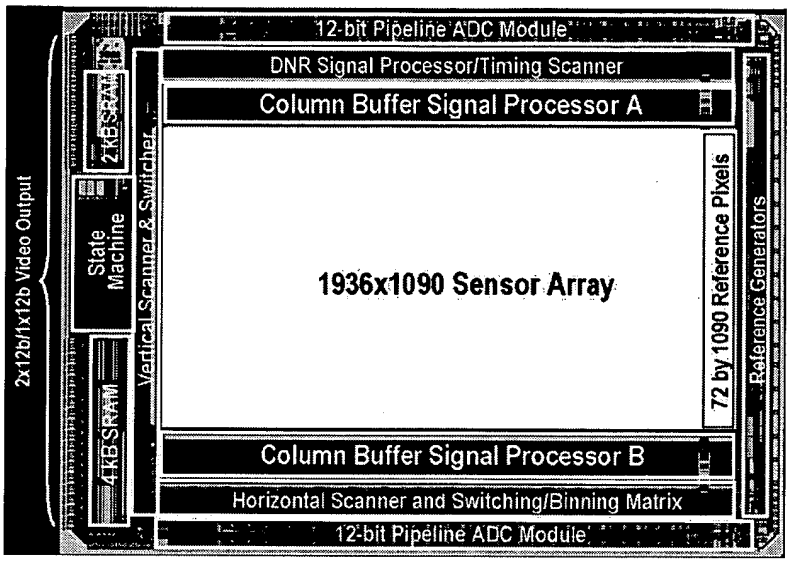

Fig. 8. Floor plan layout of 1920 × 10 CMOS sensor for HDTV.

column buffers, and pixel kTC noise suppression by means of SoC implementation of photodiode reset via distributed negative feedback. Power dissipation without digital signal processing is ~550 mW for 1080p60 (i.e., 1920 × 1080 at 60 Hz progressive) imaging.

The sensor's nominal analog and end-to-end conversion gains are 32 μV/e− and 12.2 e−/DN, respectively. Programmable analog gain of up to 48 dB is available. As-drawn fill factor for the 3T pixel with photodiode is 50%; with microlens array having 0.4-μm interpixel gap the effective fill factor is ~75% after accounting for losses at the optical interfaces of the planarized 4-metal/1-poly stack.

A. Random Noise

The SoC sensor supports several reset modes including hard reset, soft reset, tapered reset, and various combinations. Table V compares the measured to the predicted values for several key reset modes along with the concomitant image lag at 18 dB gain. Tapered reset operation at 18 dB analog gain yields minimum random noise of 8 e− with image lag <0.012%. The current methodology for HDTV cameras resets the pixel within an epoch of ~ 10 μs; using tapered reset the noise is thus ≈1/4th the predicted kTC level of 30 e− for 5.5 fF detector capacitance at 23 °C, as shown in Fig. 9. Measured noise is flat to the maximum frequency of 225 MHz as expected when the feedback amplifier is properly tuned as predicted by the analysis.

While lowest pixel noise is measured using only soft reset, the associated image lag of 10% is unacceptable for video use. Perhaps a better alternative is to use tapered reset with either longer reset time (Tapered Reset II), or to further tune the various distributed amplifier settings to improve noise reduction efficacy since the measured data agree with the predicted noise levels.

Fig. 10 shows the measured sensor noise as a function of the signal with analog gain at 12 dB for 60 Hz and 72 Hz progressive operation. Random noise is slightly higher at about 10 e− at video frequencies of 150 MHz and 180 MHz, respectively.

B. Sensor S/N Ratio

Video signal-to-noise (S/N) ratio is often measured and specified at a prescribed level of illumination. The HDTV application specifically requires measurement at 2000 lux and f8 aperture. We measured minimum sensor S/N ratio of 52 dB using progressive read and no line-mixing to boost the signal beyond the base pixel sensitivity. This compares favorably to competing FIT CCD-based HD cameras where minimum S/N ratio for 1080i60 operation (interlaced 60 Hz video with 2-line mixing for 6 dB signal boost) is typically specified from 54 to 56 dB.

Fig. 11 compares peak SNR versus signal intensity at 1080p60 (i.e., readout of 1920 by 1080 array at 60 Hz progressive) and 1080p72. Specifically denoted in the figure are the key data points corresponding to operation at 2000 lux and f8. The signal in the absence of light is set by the black clamp circuit to about 64 DN out of the 12-bit dynamic range of 4096 DN.

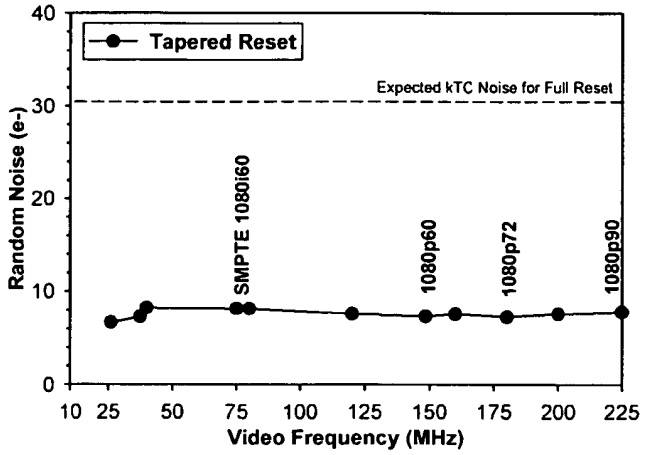

Fig. 9. Measured random noise versus sensor video frequency for various TV modes.

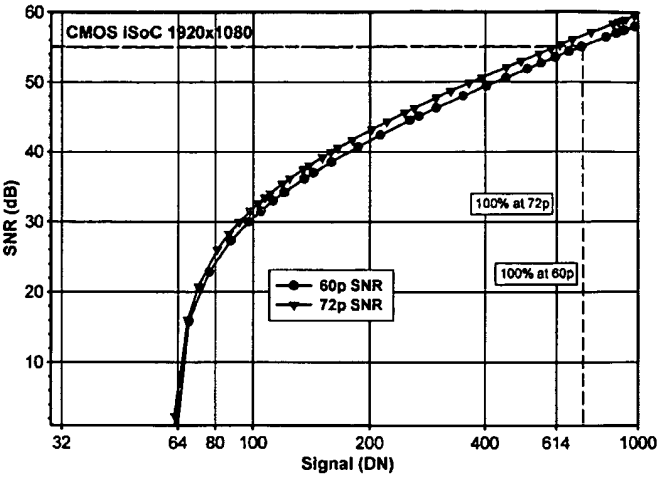

Fig. 11. Video S/N ratio at 12 dB gain with tapered reset at 2000 lux and f8 illumination.

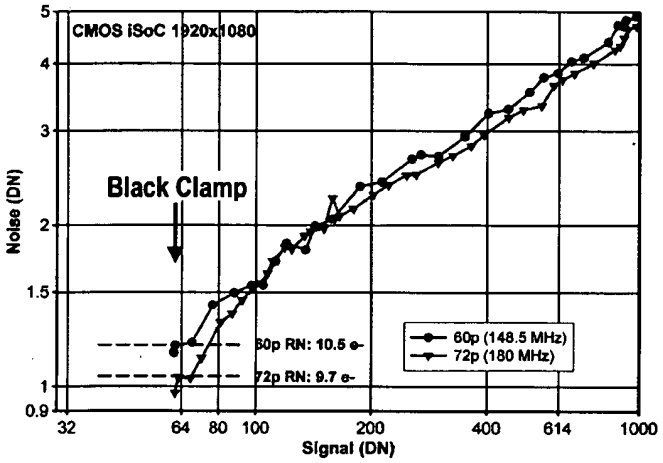

Fig. 10. Noise at 12 dB gain with tapered reset.

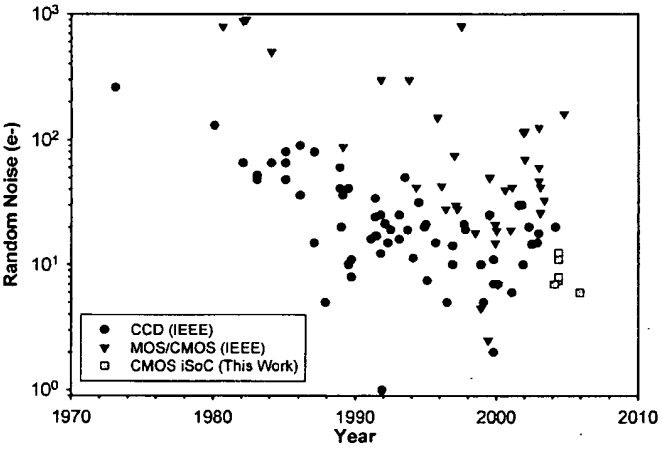

Fig. 12. Image random sensor noise in IEEE publications.

V. Comparison of Noise Performance

The sensor's random noise levels are compared to other sensors in Fig. 12, a compilation of noise and video frequency data from IEEE papers since the early 1970s. The measured sensor read noise is comparable to CCD noise at lower operating frequencies. Random noise levels for recent CCDs are arguably higher due to higher pixel density and higher video frequency per output tap as previously shown [14].

Since random noise typically increases with frequency at 3 dB per octave for CCD sensors [15], the HD CMOS sensor's noise levels are arguably better judged by using a metric that normalizes random noise to the video frequency so that the workaround of using additional video taps can be directly compared to the CMOS sensor. The figure of merit, ρ, is simply the random noise in electrons divided by the square root of the sensor's video frequency. Fig. 13 plots ρ versus sensor frequency for the database assimilated in Fig. 11. The HD CMOS sensor's measured ρ's are 8.7×10^{-4} e $-/\sqrt{\text{Hz}}$ at 75 MHz (1080/30 p), 6.5×10^{-4} and 9.8×10^{-4} at 150 MHz (1080/60 p), 9.3×10^{-4} at 180 MHz (1080/72 p), and 7.3×10^{-4} e $-/\sqrt{\text{Hz}}$ at 225 MHz (1080/90 p). Though

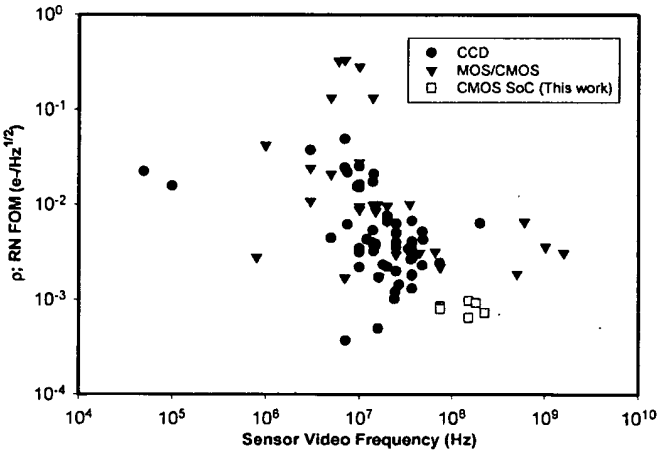

Fig. 13. Normalized figure-of-merit ρ versus sensor video frequency for various image sensors.

astronomy and low-light-level CCDs using either high-gain output amplifiers [16] or shift registers with avalanche gain [17] achieve ~1 e− read noise, their lower useful video rates yield higher values of the normalized metric ρ.

VI. Conclusion

We report a SoC technique for suppressing kTC noise that is used in a progressive 2/3-inch 1920 × 1080 sensor to generate 12-bit video with <10 e- read noise and 2.2 V/lux-s sensitivity at up to 90 Hz frame rate. S/N ratio is >52 dB at standard scene illumination (2000 lux, f8 and 89% reflectivity). Minimum random noise at 18 dB gain is 8 e-, independent of video frequency, using a SoC technique to minimize noise. Maximum frame rate for contiguous 1280 × 720 region-of-interest is 180 Hz at SNR of 52 dB. Analog and digital signal processing limit fixed pattern noise to <1.8 DN. Minimum horizontal modulation transfer function (MTF) for 625 nm illumination is 50% at Nyquist.

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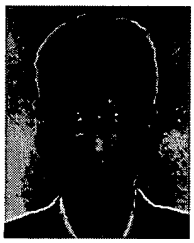
Mr. Kozlowski is a member of the IEEE Electron Devices Society, SMPTE, and SPIE.



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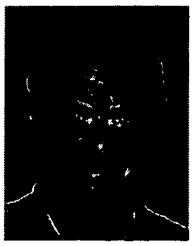

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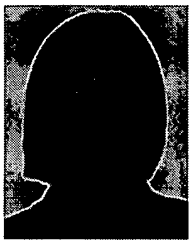

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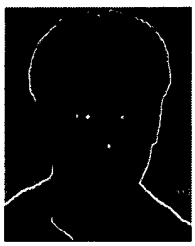

Gregory Chow received the B.A.Sc. degree in engineering physics, electrical option, from the University of British Columbia, Vancouver, BC, Canada.

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John Richardson, photograph and biography not available at the time of publication.

David Standley, photograph and biography not available at the time of publication.